REMARKS

In general, it should be noted that the structures of claims 1, 2, 3 and 7 and any claim that does not specifically mention EEPROM can also be used as EPROM non volatile memory.

REMARKS AS TO AMENDMENTS TO CLAIM 1

Claim 1 was rejected for indefiniteness on grounds the use of the term "overlie" or "overlying" in defining the floating gate structure was deemed to be indefinite. In response to this rejection, the amendments to claim 1 which are in italics in the marked up version of the claim were made. The first set of amendments defined the terms lateral and vertical with reference to the top surface of the substrate (extend laterally) and the depth of the substrate (extends vertically). The second set of amendments defines that the well is etched vertically and has one or more walls and defines the edges of the well as being coincident with these walls. This set of amendments also defines the channel and drain regions as forming a portion of the one or more walls of said well although the source region also forms a portion of the one or more walls because the well is etched down through the channel and drain layers and at least partially into the source regions. The clause "one or more walls" is used because if the well is circular, it could be defined as having only one wall, but it will have four walls and a bottom if the well is square. Square is the preferred embodiment because more devices can be packed into a given surface area on a wafer. The last set of amendments remove the term "overlying" and substitute a definition of the position of the floating gate as being laterally adjacent to the portion of the wall or walls of the well formed by the channel region such that differing levels of trapped charge in the floating gate will affect the conductivity of the channel region and the threshold voltage of the vertical MOS transistor. The term laterally adjacent means that the floating gate is adjacent in the lateral direction, *i.e.*, the direction

of the normal to the wall portion of the well formed by the intersection of the well with the channel region. The normal is as defined in the mathematical sense and is a line orthogonal to the plane of the surface of the wall of the well. If the well is round, the normal will be the orthogonal axis of a small enough portion of the curved wall with the small portion being small enough to be essentially flat and located at approximately the center of the wall intersection with the channel region.

Claim 1 was also rejected for obviousness over the combination of Yoshida et al. in view of Hsue et al., Sung et al. and Otani et al. An obviousness rejection based upon a combination of references is only proper if there is some suggestion to combine the references. Suggestion arises from a perception by those skilled in the art of a liklihood of success in solving the problem the invention solved by making the combination. To establish a prima facie case of obviousness, the PTO must show some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. There is no suggestion to combine, however, if a reference teaches away from its combination with another source. Tec Air Inc. v. Denso Manufacturing Michigan, Inc., 192 F.3d 1353; 52 USPQ2d 1294 (Fed. Cir. 1999). Technical incompatibility or any other technical problems such as inoperativeness of one of the references or impossibility to make the structure of one of the references which would render the combination inoperative or impossible to make negates suggestion. This is because those skilled in the art would not perceive a liklihood of success in making the combination because they know it either would not work or could not physically be built. In the words of the Federal Circuit from the Tec Air opinion, cited *supra*,

> A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set

> out in the reference, or would be led in a direction divergent from the path taken by the applicant, or it it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant. If when combined, the references would produce a seemingly inoperative device, then they teach away from their combination.

192 F.3d at 1360

In the obviousness rejection, the examiner takes the position that self aligned as that term is used with reference to the floating gate means no portion of the floating gate is on the horizontal surface of the substrate or the horizontal surface at the bottom of the well. This is correct.

However, for the Examiner's prima facie obviousness rejection to be valid based upon a combination of the Yoshida et al. patent in view of Hsue et al., Sung et al. and Otani et al., there must be suggestion to one skilled in the art that the results of the claimed invention can be achieved by combining the teachings of the references. Where one skilled in the art would perceive that the principal reference (Yoshida et al.) cannot be built, such a worker would not believe combining Yoshida et al. with any other reference would be productive and suggestion would not exist. In such a case, the proper course would be withdraw the oviousness rejection.

Enclosed herewith is evidence in the form of a Rule 132 declaration of Ashok Kapoor that proves that the structures of the Yoshida et al. Figures 3 and 5 cannot be built. More specifically, it was impossible to build with the processes that existed when the Yoshida et al. patent was filed and it is still impossible to build with today's processes.

The Examiner takes the position that the Yoshida et al. cover figure floating gate also is self aligned as that term is used in the claim since it has no portion on the

horizontal surface of the substrate or the horizontal surface at the bottom of the well. That is true that Yoshida et al. teach that, but this reference cannot be used for that teaching in the combination because those skilled in the art would not believe that the Yoshida et al. structure can be built. And they would be right.

The main reason why persons skilled in the art would not believe that the cover figure structure taught by Yoshida et al. could not be built is because the conductive material of the floating gate 4 sticks up above the top surface of the substrate. Yoshida et al., contrary to the requirements of 35 USC Section 112, do not teach how this structure could be built. Further, the evidence submitted herewith proves that at least one person of a very high level of skill in the art does not know how to build the Yoshida et al. structures using the processes known in the prior art and does not believe it can be built at all by anybody.

This lack of belief in the possibility of building the Yoshida et al. structure would discourage persons skilled in the art from following the path set out in the Yoshida et al. reference. This impossibility teaches away from the combination and negates the correctness of the obviousness rejection. The impossibility of building a structure which a floating gate that sticks up above the top level of the substrate suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant, *i.e., a dense EEPROM structure achieved by using a vertically oriented MOS EEPROM device with a self aligned floating gate that does not need a mask to define it thereby allowing the devices to be placed closer together on the chip.*

Because the Yoshida et al. structure cannot be built, this suggests a lack of probability of success in combining the teachings of Yoshida et al. with any of the other references to achieve the result sought by the applicant. This teaches away from

making the combination and negates suggestion thereby rendering the combination improper to support an obviousness rejection.

The Examiner is respectfully requested to withdraw the obviousness rejections based upon any combination of Yoshida et al. with any other reference.

REMARKS AS TO CHANGES TO CLAIM 2

The preamble of claim 2 was changed voluntarily to specify that it now claims just a substructure in a vertical MOS transistor which is part of a nonvolatile memory cell. This amendment was made voluntarily and comprises removal of the limitations regarding the bit line and the associated insulating layer(s) since there are probably multiple ways of doing the bit line that have nothing to do with the invention. The real advantage of the invention arises from the self aligned floating gate structure which is contained in the well.

As amended, the claim covers just the source, channel and drain regions in a substrate, a well which extends down into the substrate and intersects the drain, channel and at least part of the source and a self aligned floating gate in the well and positioned laterally of the intersection of the well and the channel such that charges trapped in the floating gate will alter the threshold of the vertical MOS transistor.

Claim 2 was rejected for indefiniteness for use of the term "overlying". To obviate this rejection, the substrate clause was amended to add a frame of reference by including language that specifies that the top surface of the substrate extends laterally and the depth of the substrate extends vertically. The floating gate clause was then amended to specify that it lies laterally adjacent to the channel region and the word line clause was amended to specify that it extends down into the well so as to lie laterally adjacent to the floating gate. This should now be clear as to the positions of these two elements in the frame of reference. The modifier "laterally adjacent" in all the claims

should be understood as meaning a sufficient overlap between the conductive structures involved where the term "laterally adjacent" is used to form a sort of parallel plate capacitor comprised of the two conductive structures separated by an insulating layer. Figure 3 illustrates the parallel plate capacitor that is formed between the word line and the floating gate as C2 and the parallel plate capacitor that is formed between the floating gate and the substrate channel regions as C1. The term laterally adjacent means one conductive structure is positioned relative to the other conductive structure such that a voltage potential applied to one conductive structure affects the voltage potential of the other structure. In the case of the C1 capacitor, charges stored in the floating gate (which is laterally adjacent the channel region of the vertical MOS transistor) affects the conductivity of the laterally adjacent channel region thereby affecting the threshold of the vertical MOS transistor. Likewise, voltage on the control gate (which is laterally adjacent to the floating gate) relative to the voltage on the source region of the substrate causes tunnelling of charges into the floating gate.

Claim 2 was also rejected for obviousness on a combination of Yoshida et al. in view of Hsue et al., Sung et al. and Otani et al. The argument made above with reference to the obviousness rejection of claim 1 applies equally to claim 2 and is hereby incorporated by reference. Since the Yoshida et al. structure would be perceived as impossible to build by those skilled in the art, the obviousness rejection of claim 2 based upon any combination of Yoshida et al. with any other reference is not supported by suggestion and is improper. The applicant hereby respectfully requests that this obviousness rejection be withdrawn.

REMARKS AS TO CHANGES TO CLAIM 3

Claim 3 was rejected for indefiniteness for its use of the term "overlying" and for obviousness over a combination of Yoshida et al. (US 5,049,956) with Hsue et al. (US

5,572,656), Sung et al. and Otani et al.

A number of voluntary changes were made to the claim to improve its form and clarity. The only amendments made to the claim in response to a rejection were to add a frame of reference to the substrate clause and to spècify that the floating gate is laterally adjacent to the channel region and the control gate is laterally adjacent to the floating gate. All other changes were made voluntarily.

REMARKS AS TO CHANGES TO CLAIM 4

Claim 4 was voluntarily amended to specify that the spacer layers being referred to are the spacer insulating layers that insulate the word line from surrounding structures such as the bit line.

A new claim 7 has been added to re-express the invention in a different way than in the other claims.

New claims have also been added to claim the self aligned substructures of the floating gate, its gate insulating layer and the control gate and ONO layer that insulates

between the floating gate and the control gate. All are self aligned and need no critical masks to build in a self aligned fashion. Also included are product by process claims that claim these self aligned structures and the processes that built them.

Respectfully submitted,

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Ronald Craig Fish
Reg. No. 28,843
Tel 408 778 3624
FAX 408 776 0426

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231
on NOVEMBER 29, 2002
(Date of Deposit)

Ronald Craig Fish, President
Ronald Craig Fish, a Law Corporation
Reg. No. 28,843

APPENDIX

IN THE SPECIFICATION

A marked up copy of the substitute specification is enclosed as is a clean copy.

IN THE CLAIMS

Below is the complete claim set, marked up in those claims which have been amended.

1. (Thrice Amended-Version to show changes) A nonvolatile memory cell comprising:

a semiconductor substrate doped to have a first conductivity type so as to act as a source region of said nonvolatile memory cell, said first conductivity type being either N-type or P-type, *and having a top surface which extends laterally and a depth which extends vertically*;

a vertical MOS transistor formed by alternating, abutting N-type and P-type doped layers in said substrate which have junctions therebetween to form a [source,] channel region and a drain region of said vertical MOS transistor with said drain region having said first conductivity type and said channel region having a second conductivity type which is P-type if said first conductivity type is N-type and is N-type if said first conductivity type is P-type, said substrate forming a source region of said first conductivity type of said vertical MOS transistor, said source regions having a junction with said channel region, and wherein a well *with one or more walls* is etched vertically into said substrate through said [alternating N-type and P-type layers] channel and drain regions and at least partially into said source region such that said drain and channel regions [alternating layers] surround said well *and form at least a portion of said one or more walls of said well*, said well having a floating gate of conductive material formed therein which is self aligned to not extend laterally beyond edges of said well, *said edges being defined by said one or more walls of said well,* and insulated from said [alternating N-type and P-type layers] channel and drain regions and said substrate by a layer of [gate] insulating material, said floating gate [overlying] *being laterally adjacent to* at least *said portion of said wall of said well formed by* said channel region of said vertical MOS transistor *such that differing levels of trapped charge in said floating gate affects the conductivity of said channel region and a threshold of said vertical MOS transistor*;

a word line contact comprising a layer of conductive material formed on said

substrate so as to extend vertically down into said well and [overlie] *lie laterally adjacent to* said floating gate but be insulated therefrom by an insulation layer such that voltage applied to said control gate affects the charge on said floating gate; and

a bit line contact comprising a layer of conductive material formed on said substrate so as to be in electrical contact with [the] said drain region of said vertical MOS transistor [formed in said substrate].

2. (Thrice Amended - Version to show changes) A substructure of a vertical MOS transistor forming part of a nonvolatile memory cell comprising:

a semiconductor substrate having a top surface which extends in a lateral direction and a thickness which extends in a vertical direction and having a drain region of a first conductivity type formed therein and suitable to act as a drain of a vertical MOS transistor;

a buried layer channel region in said semiconductor substrate doped so as to have a second conductivity type having the majority of charge carriers therein of a different polarity than said first conductivity type and suitable to act as a channel of a vertical MOS transistor formed in said substrate;

a source region of said semiconductor substrate below said channel region, said source region being doped so as to have said first conductivity type and suitable to act as a source of a vertical MOS transistor;

[a recessed gate window in the form of] a well etched [in] vertically into said semiconductor substrate, said well having one or more side walls and being deep enough to penetrate through said drain region, said channel region and at least partially into said source region such that at least some portions of [the] said one or more side walls of said well are [bordered by] defined by intersections with said source, drain and channel regions;

an insulating layer covering the bottom of said well;

a gate insulating layer formed on [the] said one or more sidewalls of said well;

a self aligned floating gate comprising a conductive material formed within said well on said gate insulating layer so as to not extend beyond [the edges] said one or more of said well and positioned laterally adjacent to the intersection of said one or more side walls and said channel region such that trapped charge in said floating gate affect the conductivity of said channel regions and a threshold of said vertical MOS transistor;

an insulating layer formed over said self aligned floating gate so as to electrically isolate said floating gate from all surrounding structures[, said floating gate having a dimension suitable so as to overlie at least said channel region]; and

a word line comprising conductive material deposited so as to extend into said well far enough to [overlie at least a portion of] lie laterally adjacent to said floating gate so as to form a control gate of a vertical MOS transistor nonvolatile EEPROM structure.[; and

a second layer of insulating material formed so as to insulate at least a portion of said word line overlying said well; and

a bit line formed over said surface of said semiconductor substrate so as to make contact with at least a portion of said drain region at said memory cell but insulated from said word line by said second layer of insulating material.]

3. (Twice Amended-Version to show changes) A nonvolatile memory cell comprising:

a semiconductor substrate having a top surface which extends laterally and having a depth which extends vertically;

a vertical MOS transistor formed by a first layer of said substrate of N-type conductivity forming a drain region of said vertical MOS transistor, a second layer of said substrate of P-type conductivity [within said substrate] and vertically adjacent to and [underlying] beneath said first layer relative to [the] said top surface of said substrate [and forming] so as to form a channel region of said vertical MOS transistor, and a third layer of said substrate of N-type conductivity within said substrate and vertically adjacent to and [underlying] beneath said second layer relative to said top surface of said substrate so as to form [and forming] a source region of said vertical MOS transistor, [and] said substrate also having a well vertically etched [into said substrate] therein so as to penetrate through said first and second layers and at least partially through said third layer, said well having at least a portion of the wall or walls thereof formed by the intersection of said well with said channel regions, and said well having a floating gate of conductive material formed therein which is self aligned so as to not extend laterally beyond [edges] the wall or walls of said well, said floating gate including at least a portion thereof which lies laterally adjacent to said portion of said wall or walls of said well formed by the intersection of said well with said channel region such that

trapped charge in said floating gate affects the conductivity of said channel regions and a threshold of said vertical MOS transistor, said floating gate being [and overlying at least said second layer and] insulated by a layer of gate insulating material from said first, second and third layers;

a word line comprising a layer of conductive material formed [above said substrate] so as to extend down into said well and [overlie] have at least a portion thereof which is laterally adjacent to said floating gate but insulated therefrom by an insulation layer so as to act as a control gate for said vertical MOS transistor;

a bit line comprising a layer of conductive material formed above [the] said top surface of said substrate so as to be in electrical contact with [the surface] a portion of said first layer; and

a spacer layer of insulating material insulating said word line from said bit line.

4. (Twice amended - version to show changes) The apparatus of claim 3 wherein said memory cell is part of an array comprised of rows and columns of adjacent memory cells and wherein said bit line is formed above said first layer so as to be above the top surface of said substrate and contacts said first layer at all points that form a top surface of said first layer between spacer layers of insulating material that insulates the word lines of adjacent memory cells.

5. (Clean) The apparatus of claim 3 wherein said memory cell is part of an array comprised of rows and columns of adjacent memory cells and wherein said bit line contacts said first layer at at least some points between said spacer layers of the word lines of adjacent memory cells and runs over the top of word lines said bit line has to cross and is insulated from each said word line at the location of each said memory cell by said spacer layer.